CLAIMS

1. An equalizer comprising:

a first tapped delay line, for receiving samples of an input signal at a first series of time points,

a second tapped delay line, for receiving samples of an input signal at a second series of time points, wherein successive time points alternate between the first and second series of time points,

a first summing circuit, for forming a first output as a weighted sum of sample values from a first series of tap points in the first tapped delay line and a first series of tap points in the second tapped delay line, wherein tap points in the first series of tap points in the first tapped delay line are at delays intermediate between the delays of successive tap points in the first series of tap points in the second tapped delay line,

a second summing circuit, for forming a second output as a weighted sum of sample values from a second series of tap points in the first tapped delay line and a second series of tap points in the second tapped delay line, wherein the respective first and second series of tap points each alternate in the first and second tapped delay lines, and wherein tap points in the second series of tap points in the first tapped delay line are at delays intermediate between the delays of successive tap points in the second series of tap points in the second tapped delay line,

an output, for forming an equalizer output signal from the first output at a third series of time points, and from the second output at a fourth series of time points, wherein the third and fourth series of time points alternate.

2. An equalizer as claimed in claim 1, wherein the first tapped delay line comprises a first plurality of controllable memory elements, and the second tapped delay line comprises a second plurality of controllable memory elements, each of the controllable memory elements alternating between time periods in which its output is static and time periods in which its output may be in transition.

3. An equalizer as claimed in claim 2, wherein the controllable memory elements are controlled such that the outputs of the first series of tap points in the first tapped delay line and the first series of tap points in the second tapped delay line are static at the third series of time points, and such that the outputs of the second series of tap points in the first tapped delay line and the second series of tap points in the second tapped delay line are static at the fourth series of time points.

4. An equalizer as claimed in claim 1, wherein the first tapped delay line comprises a first plurality of track and hold circuits, and the second tapped delay line comprises a second plurality of track and hold circuits, and

wherein track and hold circuits preceding the first series of tap points in the first tapped delay line and track and hold circuits preceding the first series of tap points in the second tapped delay line are clocked by a first clock signal, track and hold circuits preceding the second series of tap points in the first tapped delay line and track and hold circuits preceding the second series of tap points in the second tapped delay line are clocked by a second clock signal, wherein the second clock signal is the inverse of the first clock signal.

5. An equalizer as claimed in claim 1 comprising:

a number N of tapped delay lines, wherein $N > 2$, for receiving samples of the input signal in sequence,

a number N of summing circuits, for forming respective outputs as weighted sums of sample values from a respective series of points arranged sequentially in the tapped delay lines,

an output, for forming the equalizer output signal from the outputs of the summing circuits sequentially.

6. An equalizer as claimed in claim 1, wherein the first tapped delay line comprises a first series of analog track and hold circuits, and the second tapped delay line comprises a second series of analog track and hold circuits.

7. An equalizer as claimed in claim 1, wherein the first tapped delay line comprises a first series of digital sample and hold circuits, and the second tapped delay line comprises a second series of digital sample and hold circuits.

8. An equalizer as claimed in claim 1, in the form of a decision feedback equalizer, further comprising:

decision circuits for forming first and second binary outputs from the first and second outputs,

a second part of said first tapped delay line, for receiving the first binary output as an input thereto,

a second part of said second tapped delay line, for receiving the second binary output as an input thereto,

wherein the first summing circuit forms the first output as a weighted sum of sample values from a first series of alternate points in the first tapped delay line including the second part of said first tapped delay line and a first series of alternate points in the second tapped delay line including the second part of said second tapped delay line, and

wherein the second summing circuit forms the second output as a weighted sum of sample values from a second series of alternate tap points in the first tapped delay line including the second part of said first tapped delay line and a second series of alternate tap points in the second tapped delay line including the second part of said second tapped delay line.

9. An equalizer as claimed in claim 8, wherein the first tapped delay line comprises a first plurality of controllable memory elements, and the second tapped delay line comprises a second plurality of controllable memory elements, each of the controllable memory elements alternating between time periods in which its output is static and time periods in which its output may be in transition.

10. An equalizer as claimed in claim 9, wherein the controllable memory elements are controlled such that the outputs of the first series of tap points in the first tapped delay line and the first series of tap points in the second tapped delay line

are static at the third series of time points, and such that the outputs of the second series of tap points in the first tapped delay line and the second series of tap points in the second tapped delay line are static at the fourth series of time points.

11. An equalizer as claimed in claim 8, wherein the first tapped delay line comprises a first plurality of track and hold circuits, and the second tapped delay line comprises a second plurality of track and hold circuits, and

wherein track and hold circuits preceding the first series of tap points in the first tapped delay line and track and hold circuits preceding the first series of tap points in the second tapped delay line are clocked by a first clock signal, track and hold circuits preceding the second series of tap points in the first tapped delay line and track and hold circuits preceding the second series of tap points in the second tapped delay line are clocked by a second clock signal, wherein the second clock signal is the inverse of the first clock signal.

12. An equalizer comprising a plurality of tapped delay lines, for receiving received sample values in sequence, and a corresponding plurality of summing circuits, such that an output signal is formed from an output of each of the plurality of summing circuits in sequence.

13. An equalizer, comprising:

an input, for demultiplexing alternate samples of a received signal into first and second data streams;

a first tapped delay line, connected to receive the first data stream, and comprising a first plurality of controllable memory elements;

a second tapped delay line, connected to receive the second data stream, and comprising a second plurality of controllable memory elements; and

an output,

wherein each of the controllable memory elements alternates between time periods in which its output is static and time periods in which its output may be in transition,

wherein the controllable memory elements in the first tapped delay line are alternately members of a first group of controllable memory elements whose outputs are static during first time periods and may be in transition during second time periods, alternating with the first time periods, and a second group of controllable memory elements whose outputs are static during second time periods and may be in transition during first time periods,

wherein the controllable memory elements in the second tapped delay line are alternately members of a third group of controllable memory elements whose outputs may be in transition during first time periods and are static during second time periods, and a fourth group of controllable memory elements whose outputs are static during first time periods and may be in transition during second time periods, and

wherein the output receives a weighted sum of the outputs of the controllable memory elements of the first and fourth groups during first time periods, and receives a weighted sum of the outputs of the controllable memory elements of the second and third groups during second time periods.

14. An equalizer as claimed in claim 13, wherein the output comprises a first summing circuit for forming the weighted sum of the outputs of the controllable memory elements of the first and fourth groups, and a second summing circuit for forming the weighted sum of the outputs of the controllable memory elements of the second and third groups, and wherein the output is adapted to supply the output of the first summing circuit as an output during first time periods and to supply the output of the second summing circuit as an output during second time periods.

15. An equalizer as claimed in claim 13, comprising means for supplying a clock signal to the controllable memory elements of the first and fourth groups, and for supplying an inverted clock to the controllable memory elements of the second and third groups.

16. An equalizer as claimed in claim 13, wherein the controllable memory elements comprise analog track and hold circuits.

17. An equalizer as claimed in claim 13, wherein the controllable memory elements comprise digital track and hold circuits.

18. An optical receiver, comprising:

means for converting a received optical signal to an electronic signal; and

an equalizer as claimed in any preceding claim, connected to receive the electronic signal as an input thereto.